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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,356	01/23/2004	Won-Jun Lee	9898-314	7097

20575 7590 02/13/2006

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EXAMINER	
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ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/13/2006

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10/763,356	1/23/04	Won-Jun Lee	9898-314

EXAMINER

ART UNIT	PAPER
0206	

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Attached, please find an English translation for KR 2002-90452. Note figures 5e and 7d.

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Art Unit: 1765

PTO 06-2031

Korean Laid-Open Patent
No. 2002-0090452

SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURE THEREOF

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UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. JANUARY 2006
TRANSLATED BY THE MCELROY TRANSLATION COMPANY

KOREAN INTELLECTUAL PROPERTY OFFICE
PATENT JOURNAL (A)
LAID-OPEN PATENT NO. 2002-0090452

Int. Cl.[7]:	H 01 L 27/10
Filing No.:	10-2001-0029008
Filing Date:	May 25, 2001
Publication Date:	December 5, 2002
Examination Request:	Not filed

SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURE THEREOF

[Bandochei memori soja mip kuejaezo bangbeop]

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Applicant:	Samsung Electronics Co., Ltd.

[There are no amendments to this patent.]

Specification /2*

Brief description of the figures

Figure 1 is a cross section showing a semiconductor memory device having a storage node electrode with a generally concave shape.

Figure 2 is a cross section showing the semiconductor memory device of Application Example 1 of the present invention.

Figure 3a is a plan view showing a storage node electrode cell.

Figure 3b is a cross section development diagram showing the storage node electrode of Application Example 1 of the present invention.

Figure 4 is a graph showing the surface area of a height reduction portion of the storage node electrode.

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* [Numbers in the right margin indicate pagination of the original foreign text.]

Figures 5a-5e are cross sections of each process for explaining the method for manufacturing the semiconductor memory device of Application Example 1 of the present invention.

Figure 6 is a cross section showing the semiconductor memory device for explaining Application Example 2 of the present invention.

Figures 7a-7d are cross sections of each process for explaining the method for manufacturing the semiconductor memory device of Application Example 2 of the present invention.

Figure 8a is a graph showing the wet-etching rate of a sacrificial film with respect to the plasma vapor deposition power of the sacrificial film.

Figure 8b is a graph showing the wet-etching rate of the sacrificial film with respect to the vapor deposition temperature of the sacrificial film.

Figure 8c is a graph showing the wet-etching rate of the sacrificial film with respect to the rate of a nitric acid (N_2O) gas to a silane (SiH_4) gas constituting the sacrificial film.

Figure 8d is a graph showing the wet-etching rate of the sacrificial film with respect to the distance between a shower head and a substrate of a semiconductor equipment constituting the sacrificial film.

Figure 8e is a graph showing the wet-etching rate of the sacrificial film with the respect to the vapor deposition pressure of the sacrificial film.

Explanation of numerals of the main parts of the figures:
26, 30 Storage node electrodes

Detailed explanation of the invention

Objective of the invention

Technical field of the invention and prior art of the field

The present invention pertains to a semiconductor memory device and its manufacturing method. More specifically, the present invention pertains to a storage node electrode of a semiconductor memory device and its manufacturing method.

Along with the high integration of semiconductor devices, the area occupied by a unit cell is reduced. On the other hand, the driving performance of DRAM is determined by the capacitance of a capacitor, various efforts of increasing the capacitance are continued, in spite of the reduction of the area occupied by the capacitor. As a part of these effectors, a storage node /3
electrode is cubically formed as a concave type, cylinder type, fin type, or box type to increase the effective area of the storage node electrode of the capacitor. Among them, the concave-type storage node electrode is easily flattened, and problems such as oxidation due to an inferior

alignment are generated less, so that the concave type is frequently used in current high-integrated memory devices.

Here, a semiconductor memory device having a general concave-type storage node electrode is explained referring to Figure 1.

As shown in Figure 1, an interlayer insulating film (12) is formed in the upper part of a semiconductor substrate (10) equipped with a circuit device (not shown in the figure) such as a MOS transistor. Storage node contacts (14) are provided to the inside of the interlayer insulating film (12). As is well known, the storage node contacts (14) connect a source area (not shown in the figure) of a selected MOS transistor and a storage node electrode being formed later. Concave storage node electrodes (16) with a cup shape are formed in a prescribed part of the upper part of the storage node contacts (14) and the interlayer insulating film (12). The concave-type storage node electrodes (16) are formed by the following method. First, a sacrificial oxide film (not shown in the figure) with a prescribed thickness is vapor-deposited onto the upper part of the interlayer insulating film (12) that includes the storage node contacts (14). Next, openings are formed by patterning the sacrificial film so that the storage node contacts (14) can be exposed. Then, an electroconductive layer (not shown in the figure) and an insulating film (not shown in the figure) for a node separation are formed in the upper part of the sacrificial film so that they may be contacted with the exposed storage node contacts (14). The electroconductive layer and the insulating film for a node separation are subjected to a chemical and mechanical polishing (hereinafter, called CMP). Then, the insulating film for a node separation and the sacrificial film are removed by a well-known method, so that the concave-type storage node electrodes (16) are formed.

However, along with the increase of the degree of integration of the current semiconductor memory devices, the pitch size of wirings and the distance (D) between the storage node electrodes (16) should be reduced in consideration of the degree of integration, whereas the height of the storage node electrode should be relatively increased to obtain a high capacitance. At that time, if the height of the storage node electrode is increased, since the aspect ratio is increased, a dielectric film and an upper electrode are not easily vapor-deposited, and if the height of the storage node electrode is maintained, as is conventional, a desired capacitance is difficult to obtain.

Also, if the distance (D) between the storage node electrodes (16) is reduced in consideration of the wiring pitch, an interference phenomenon with the adjacent storage node electrodes, such as cross-linking, is generated.

Technical problems to be solved by the invention

Therefore, the technical objective to be achieved by the present invention is to provide a semiconductor memory device that can reduce the interference with adjacent storage node electrodes while reducing the gap between the storage node electrodes.

Also, another technical objective to be achieved by the present invention is to provide a semiconductor memory device that can secure a sufficient capacitor.

Also, another technical objective to be achieved by the present invention is to provide a method for manufacturing the above-mentioned semiconductor memory device.

Constitution and operation of the invention

The objectives of the present invention, the other purposes, and new characteristics will be clarified by the description of this specification and the attached figures.

The outline of the representative characteristics of the invention presented in this application is briefly explained as follows. First, the semiconductor memory device of an embodiment of the present invention includes a semiconductor substrate having an electroconductive area and an interlayer insulating film having several storage node contacts in contact with the electroconductive area of the semiconductor substrate. Concave-type storage node electrodes are formed in the upper part of the interlayer insulating film so that they can respectively be in contact with the storage node contacts. Here, the gap between the adjacent storage node electrodes is maintained to the degree that a first length (X) is subtracted from the minimum distance (N) that does not cause a cross-link, and the height of the above-mentioned each storage node electrode is lower than a set height by approximately the value of the first length divided by two. /4

Also, the semiconductor memory device of the present invention of another application example of an embodiment of the present invention includes a semiconductor substrate having an electroconductive area and an interlayer insulating film having several storage node contacts in contact with the electroconductive area of the semiconductor substrate. In the upper part of the interlayer insulating film, concave-type storage node electrodes in contact with each of the storage node contacts are formed. At that time, the storage node electrodes have an inverted truncated cone shape the diameter of which gradually increases toward the upper part, and the shortest gap between the above-mentioned adjacent storage node electrodes is maintained to the degree that a first length (X) is subtracted from the minimum distance (N) that does not cause a cross-link, and the height of each storage node electrode is lower than a set height by approximately the value of the first length divided by two.

Also, the method for manufacturing the semiconductor memory device of another embodiment of the present invention is as follows. First, an interlayer insulating film having

storage node contacts is formed on a semiconductor substrate, and a sacrificial film is formed in the upper part of the interlayer insulating film. Next, openings are formed by etching the sacrificial film so that the storage node contacts can be exposed, and an electroconductive layer is formed in the openings and on the surface of the sacrificial film. Then, the electroconductive layer is chemically and mechanically polished so that the sacrificial film surface may be exposed, and storage node electrodes are formed by etching the electroconductive layer up to a prescribed length. At that time, at the step that forms the openings, the openings are formed so that the gap between the openings can be maintained to the degree that a first length (X) is subtracted from the minimum length that does not cause a cross-link between the storage node electrodes, and at the step that etches the electroconductive layer up to a prescribed length, the electroconductive layer is etched to the degree of the first length divided by two.

Also, in the method for manufacturing the semiconductor memory device of another application example of another embodiment of the present invention, an interlayer insulating film having storage node contacts is formed on a semiconductor substrate, and first and second sacrificial films with different wet-etching rates are sequentially formed in the upper part of the interlayer insulating film. Then, a first opening is formed by anisotropically etching the first and second sacrificial films so that the storage node contacts are exposed, and a second opening whose diameter is widened toward the upper part by wet-etching the first and second sacrificial films. Then, an electroconductive layer is formed in the second opening and on the surface of the sacrificial films, and the electroconductive layer is chemically and mechanically polished so that the sacrificial film surfaces are exposed. Then, storage node electrodes are formed by etching the electroconductive layer up to a prescribed length. The shortest gap between the second opening is preferably maintained at the gap to the degree that a first length (X) is subtracted from the minimum distance that does not cause a cross-link between the storage node electrodes, and at the step that etches the electroconductive up to a prescribed length, the electroconductive layer is etched to the degree of the first length divided by two.

Next, preferred application examples of the present invention are explained based on the attached figures.

Here, the application examples of the present invention can be modified in various shapes, and it should be interpreted that the range of the present invention is not limited to the following application examples. The application examples of the present invention are provided to a person with average knowledge in the corresponding field to further completely explain the present invention. Therefore, the shapes of elements in the figures are exaggerated to stress a more distinct explanation, and the elements indicated by the same symbols in the figures represent the same elements. Also, in case it is described that a certain layer exists "on" another layer or a semiconductor substrate, the certain layer can exist in direct contact with the

above-mentioned another layer or semiconductor layer, or a third layer can be interposed between them.

Application Example 1

Figure 2 is a cross section showing the semiconductor memory device of Application Example 1 of the present invention, Figure 3a is a plan view showing a storage node electrode cell, and Figure 3b is a cross section development diagram showing the storage node electrode of Application Example 1 of the present invention. Also, Figure 4 is a graph showing the surface area of a height reduction portion of the storage node electrode. Figures 5a-5e are cross sections of each process for explaining the method for manufacturing the semiconductor memory device of Application Example 1 of the present invention. /5

First, in Figure 2, an interlayer insulating film (22) is formed in the upper part of a semiconductor substrate (20) equipped with a MOS transistor consisting of gate, source, and drain (not shown in the figure) and other circuit devices (not shown in the figure). Storage node contacts (24) in contact with the source (not shown in the figure) of the MOS transistor are provided to the inside of the interlayer insulating film (22). Storage node electrodes (26) are formed in the upper part of a prescribed part of the storage node contacts (24) and the interlayer insulating film (22). The storage node electrodes (26) are formed in a concave shape. At that time, the gap between the storage node electrodes (26) and the adjacent storage node electrode (26) is formed at a width that is narrower than a minimum range (N) that does not cause a cross-link, by a prescribed length (X, called a first length). On the other hand, the height of the storage node electrodes (26) is formed at a level that is lower than a generally set height, that is, the height (H) that can secure a minimum capacitance in relation to a wiring pitch, by 1/2 of the first length (X/2, hereinafter, a second length).

At that time, if the height of the storage node electrode (26) is reduced by 1/2 of the distance reduction portion (X) between the storage node electrodes (26) instead of reducing the gap between the storage node electrodes (26), a substantial gap between the storage node electrodes (26) is the minimum distance (N) that does not cause a cross-link. Therefore, even if the gap between the storage node electrodes (26) is reduced, since the minimum distance (N) that does not cause a cross-link is continuously maintained, the cross-link is not generated.

Also, even if the height of the storage node electrodes (26) is reduced, since the gap between the storage node electrodes (26) is reduced, the surface area of the storage node electrodes (26) is actually increased.

It will be explained in the following in detail, through Figures 3a and 3b. First, Figure 3a shows a storage electrode cell. Here, the storage node electrode cell includes substantial storage node electrode (S) and part of an insulating area (I) for insulating the storage node electrode (S)

and the adjacent storage node electrode (not shown in the figure). Here, in case the memory device of the present invention is a 0.10 μm class DRAM device, the horizontal length of the storage node electrode cell is about 2000 Å, and the vertical length is 4000 Å. On the other hand, the minimum width of the insulating area (I) that can prevent the cross-link is 700 Å, and the minimum height is 1200 Å. In this case, when the height of the storage node electrode (26, see Figure 2) is not reduced, the surface area of the storage node electrode is as follows. Here, Å units are omitted.

Mathematical Equation 1:

$$[\{2000 - 700) + (4000 - 1200)\} \times 2 \times H] + \{(2000 - 700) \times (4000 - 1200)\}$$

On the other hand, as in this application example, when the distance of the adjacent storage node electrode (26) is reduced by the first length (X) and the height is reduced by the second length (X/2), the surface area of the storage node electrode is as follows.

Mathematical Equation 2:

$$[\{2000 - 700 + X) + (4000 - 1200 + X)\} \times 2 \times (H - X/2)] + \{(2000 - 700 + X) \times (4000 - 1200 + X)\}$$

In the comparison of the above-mentioned equations 1 and 2, even if the height is reduced by X/2, since the width is increased by X for each surface in the entire surface area, a substantial surface area is much more increased, compared with the prior art.

The graph is Figure 4 is based on this result, and shows the surface area of the storage node electrode with respect to the first length (X) when the set height (H) of the storage node electrode was changed, a graph showing. According to Figure 4, when the set height (H) of the storage node electrode was changed to 8000Å, 9000Å, 11,000 Å, and 12,000Å, respectively, the surface area was increased with the increase of the first length (X).

Also, the method for manufacturing the storage node electrode of the above-mentioned /6
semiconductor memory device is explained referring to Figures 5a-5e.

First, in Figure 5a, an interlayer insulating film (20) is formed in the upper part of a semiconductor substrate (20) equipped with a MOS transistor consisting of gate, source, and drain (not shown in the figure) and other circuit devices (not shown in the figure). At that time, the interlayer insulating film (20) can include a flattened film, and in some cases, a bit line (not shown in the figure) may be buried in the interlayer insulating film (20). Storage node contact holes (st) are formed by etching the interlayer insulating film (20) so that the source (not shown in the figure) of a selected MOS transistor is exposed. Then, an electroconductive layer is vapor-deposited onto the upper part of the interlayer insulating film (20) so that the storage node contact holes (st) are sufficiently buried. Then, storage node contacts (24) are formed by

removing the electroconductive layer by a CMP method so that the interlayer insulating film (22) is exposed.

Next, referring to Figure 5b, a sacrificial film (25) is vapor-deposited onto the upper part of the interlayer insulating film (22) and the storage node contact (24). At that time, the sacrificial film (25) is generally vapor-deposited at a thickness of an approximate set storage-node-electrode height (H) in consideration of the wiring pitch and the design rule. At that time, an etching-retardation film (not shown in the figure) may be formed in the upper part of the sacrificial film (25). At that time, if the etching-retardation film is formed, the total thickness of the sacrificial film (25) and the etching-retardation film is the set storage-node-electrode height (H). In addition, the sacrificial film (25) must be formed of a substance that will later constitute the storage node electrode and that has an excellent etching selection ratio, and, if a separate etching-retardation film is not used, a substance with an excellent polishing selection ratio.

Referring to Figure 5c, openings (OP) are formed by patterning a prescribed part of the sacrificial film (25) or etching-retardation film so that a prescribed part of the storage node contact (24) may be exposed. At that time, the distance between the adjacent openings (OP) is preferably a size that is smaller than the minimum distance (N) that does not cause a cross-link, by the first length (X).

As shown in Figure 5d, an electroconductive layer (260) for the storage node electrode is vapor-deposited at a prescribed thickness on the surface of the sacrificial film (25) in which the openings (OP) are formed. At that time, the electroconductive layer (260) is vapor-deposited at a thickness to the degree that it can be covered along the surface of the openings (OP) while not burying the openings (OP). After vapor-depositing an insulating film for a node separation (not shown in the figure) on the upper part of the electroconductive layer (260), the electroconductive layer (260) for the storage node electrodes and the insulating film for a node separation (not shown in the figure) are subjected to the CMP until the sacrificial film (25) or etching-retardation film (not shown in the figure) is exposed.

Then, as shown in Figure 5e, after removing the insulating film for a node separation by a well-known method, storage node electrodes (26) are formed by etching the electroconductive layer (260) as much as 1/2 of the first length (X), that is, the second length (X/2). Then, the sacrificial film (25) is removed by a well-known wet-etching method. Thus, the storage node electrodes (26) having a concave shape and a height reduced by the second length (X/2) are completed.

According to this application example, the gap between the adjacent storage node electrodes is reduced by a prescribed length from the minimum length that does not cause a cross-link, and the height of the storage node electrodes is reduced by 1/2 of the reduced length. Thus, a substantial gap between the storage node electrodes maintains approximately the

minimum length that does not cause a cross-link. Thereby, the cross-link is not generated while reducing the gap between the storage electrodes. In addition, the diameter of the storage electrodes is increased, so that not only is the surface area increased, but the height of the storage node electrodes is reduced, thereby largely reducing the aspect ratio.

Application Example 2

Figure 6 is a cross section showing the semiconductor memory device for explaining /7
Application Example 2 of the present invention, and Figures 7a-7d are cross sections of each process for explaining the method for manufacturing the semiconductor memory device of Application Example 2 of the present invention. Also, Figure 8a is a graph showing the wet-etching rate of a sacrificial film with respect to the plasma vapor-deposition power of the sacrificial film, and Figure 8b is a graph showing the wet-etching rate of the sacrificial film with respect to the vapor deposition temperature of the sacrificial film. Also, Figure 8c is a graph showing the wet-etching rate of the sacrificial film with respect to the rate of a nitric acid (N_2O) gas to a silane (SiH_4) gas constituting the sacrificial film. Figure 8d is a graph showing the wet-etching rate of the sacrificial film with respect to the distance between a shower head and a substrate of a semiconductor equipment constituting the sacrificial film. Figure 8e is a graph showing the wet-etching rate of the sacrificial film with the respect to the vapor-deposition pressure of the sacrificial film.

In addition, the same explanation for the same parts as those of the above-mentioned Application Example 1 is excluded from this application example.

First, referring to Figure 6, the distance between a storage node electrode (30) of this application example and its adjacent storage node electrode (30) is formed at a size which is narrower than the minimum length (N) that does not cause a cross-link, by a first length (X), and its height is formed at a level that is lower than a set length (H) by a second length (X/2) which is a reduction of the first length (X) by 1/2. In addition, the storage node electrode (28) of this application example has an inverted truncated cone shape the diameter of which is gradually increased toward the upper part while having a concave shape with a structure more stable than that of the above-mentioned Application Example 1. At that time, the shortest distance between the adjacent storage node electrodes (30) is narrower than the minimum distance (N) that does not cause a cross-link, by the first length (X).

With the formation of the storage node electrodes (30) in this manner, since the height is reduced by the second length similarly to the above-mentioned Application Example 1, problems such as cross-linking are not generated, even if the gap between the adjacent storage node electrodes (30) is reduced. Rather the area of the storage node electrodes (30) is increased with the decrease of the gap between the storage node electrodes (30), so that not only can a

large-capacity capacitance be secured, but the step difference of the storage node electrodes (30) is reduced.

In addition, in this application example, with the formation of the storage node electrodes (30) with an inverted truncated cone shape, structurally unstable problems can be solved, and the formation of subsequent dielectric film and plate electrode is made easy.

The method for manufacturing the semiconductor memory device having the storage node electrodes of this application example will be explained in detail, referring to Figures 7a-7d.

First, as shown in Figure 7a, a first sacrificial film (250a) and a second sacrificial film (250b) are sequentially vapor-deposited onto the upper part of an interlayer insulating film (22) in which storage node contacts (24) are formed. Here, the second sacrificial film (250b) is formed by a substance with a wet-etching selectionratio higher than that of a first sacrficial film (250a). At that time, the wet-etching ratio of the first and second sacrificial films (250a, 250b) can be regulated by vapor-deposition power, vapor-deposition temperature, vapor-deposition gas ratio, vapor-deposition pressure, etc.

In other words, as shown in Figure 8a, the first sacrificial film (250a) is vapor-deposited while applying a vapor deposition plasma power (W) of 250-300 W, for instance, and the second sacrificial film (250b) is vapor-deposited while applying the vapor deposition plasma power (W) of about 100-150 W. Thus, in the subsequent wet-etching process, for the same wet-etching solution, the first sacrificial film (250a) is etched at a wet-etching rate of 2300 Å/min or less, whereas the second sacrificial film (250b) is etched at a wet-etching rate of about 3000 Å/min or more.

Also, as shown in Figure 8b, when the first sacrificial film (250a) is vapor-deposited at a temperature of 400-450°C and the second sacrificial film (250b) is vapor-deposited at a temperature of 270-300°C, the wet-etching selection ratio between the first sacrificial film (250a) and the second sacrificial film (250b) is also distinct.

As shown in Figure 8c, when the ratio of a nitric acid gas to a silane gas is regulated to about 0.02-0.03% during the vapor deposition of the first sacrificial film (250a) and the ratio of the nitric acid gas to the silane gas is regulated to about 0.05-0.06% during the vapor deposition of the second sacrificial film (250b), the wet-etching selection ratio between the first sacrificial film (250a) and the second sacrificial film (250b) is also distinct.

As shown in Figure 8b, during the vapor deposition of the first sacrificial film (250a), /8
the distance between a shower head (not shown in the figure) for jetting a vapor-depositing gas in a semiconductor vapor deposition equipment and the semiconductor substrate is regulated to 200-250 mils, and during the vapor deposition of the second sacrificial film (250b), the distance between the shower head and the semiconductor substrate is regulated to about 400-450 mils.

With the vapor deposition in this manner, the wet-etching selection ratio between the first sacrificial film (250a) and the second sacrificial film (250b) is also distinct.

Also, as shown in Figure 8e, the first sacrificial film (250a) is vapor-deposited at a pressure of 1-1.5 torr, and the second sacrificial film (250b) is vapor-deposited at a pressure of 3-5 torr. With the vapor deposition in this manner, the wet-etching selection ratio between the first sacrificial film (250a) and the second sacrificial film (250b) is distinct.

At that time, each sacrificial film (250a, 250b) is generally vapor-deposited at a thickness of an approximate set storage-node-electrode height (H) in consideration of the wiring pitch and the design rule. At that time, an etching-retardation film (not shown in the figure) may be formed in the upper part of the second sacrificial film (250b). In this case, the total thickness of each sacrificial film (250a, 250b) and the etching-retardation film is approximately the set storage-node-electrode height (H). In addition, each sacrificial film (250a, 250b) is preferably formed of a substance that constitutes the storage node electrodes and has an excellent etching selection ratio, or if a separate etching-retardation film is not used, a substance with an excellent polishing selection ratio.

Then, referring to Figure 7a, if the first and second sacrificial films (250a, 250b) or etching-retardation film are formed so that a prescribed part of the storage node contacts (24) may be exposed, openings (OP) are formed by patterning a prescribed part of the first and second sacrificial films (250a, 250b) or etching-retardation film. At that time, the distance between the adjacent openings (OP) is set to a size that is slightly greater than the value in which the first length (X) is subtracted from the minimum distance (N) that does not cause a cross-link, in consideration of the subsequent additional wet-etching. Thus, the photolithography process for forming the openings (OP) is easier than that of the above-mentioned Application Example 1. In addition, the etching of the first and second sacrificial films (250a, 250b) for forming the openings (OP) is advanced by an anisotropic etching method.

Next, as shown in Figure 7b, the first and second sacrificial films (250a, 250b) are wet-etched so that the shape of the openings (OP) may be an inverted truncated cone, that is, the side walls of the openings may be sloped. At that time, compared with the first sacrificial film (250a), since the second sacrificial film (250b) has a high wet-etching rate, the diameter of the openings (OP) is further increased toward the upper part. This wet-etching process is advanced until the gap between the adjacent storage node electrodes reaches the value in which the first length (X) is subtracted from the minimum length that does not cause a cross-link.

Next, as shown in figure 7c, an electroconductive layer (300) for the storage node electrodes is vapor-deposited onto the upper part of the sacrificial films (250) in which the openings (OP) have sloped side walls, and an insulating film (32) for a node separation is vapor-deposited onto the upper part of the electroconductive layer (300). Then, if the second

sacrificial film (250b) or etching-retardation film is formed, the insulating film (32) for a node separation and the electroconductive layer (300) are subjected to the CMP so that the etching-retardation film can be exposed.

Then, referring to Figure 7d, the insulating film (32) for a node separation is removed according to the well-known removal method, and the height of the electroconductive layer (300) is etched by each second length (X/2), so that the storage node electrodes (30) are formed.

Thus, since the photolithography process for forming the openings is easy, the storage node electrodes of this application example is stable in terms of process. In addition, since the storage node electrodes are formed in an inverted truncated shape the diameter of which is gradually increased toward the upper part, the storage node electrodes can be more stably formed.

Effects of the invention

As explained above in detail, according to Application Example 1 of the present invention, the gap between the adjacent storage node electrodes is further reduced by the minimum distance that does not cause a cross-link, by a prescribed length, and the height of the storage node electrode is reduced by 1/2 of the reduced distance. Thus, a substantial gap between the storage node electrodes maintains approximately the minimum distance that does not cause a cross-link. Thus, the cross-link is not generated while reducing the gap between the storage electrodes. In addition, the diameter of the storage electrodes is increased, so that not only is the surface area increased, but the height of the storage node electrodes is reduced, thereby largely reducing the aspect ratio. /9

Also, according to Application Example 2 of the present invention, the storage node electrodes are formed so that the diameter of the storage node electrodes can be gradually widened toward the upper part. Thus, the storage node electrodes are more stably formed.

In addition, the present invention can be variously modified and applied in the range where its essence is not deviated.

Claims

1. A semiconductor memory device, characterized by the fact that included in a semiconductor memory device, is a semiconductor substrate having an electroconductive area, an interlayer insulating film that is formed in the upper part of the above-mentioned semiconductor substrate and has several storage node contacts in contact with the electroconductive area of the above-mentioned semiconductor substrate, and concave-type storage node electrodes being formed in the upper part of the interlayer insulating film while being contacted with each of the above-mentioned storage node contacts; the gap between the

above-mentioned adjacent storage node electrodes is maintained to the degree that a first length (X) is subtracted from the minimum distance (N) that does not cause a cross-link; and the height of each above-mentioned storage node electrode is lower than a set height by approximately the value of the first length divided by two.

2. A semiconductor memory device, characterized by the fact that in a semiconductor memory device, it includes a semiconductor substrate having an electroconductive area, an interlayer insulating film that is formed in the upper part of the above-mentioned semiconductor substrate and has several storage node contacts in contact with the electroconductive area of the above-mentioned semiconductor substrate, and concave-type storage node electrodes being formed in the upper part of the interlayer insulating film while in contact with each of the above-mentioned storage node contacts; the above-mentioned storage node electrodes have an inverted truncated cone shape whose diameter gradually increases toward the upper part; the shortest gap between the above-mentioned adjacent storage node electrodes is maintained to the degree that a first length (X) is subtracted from a minimum distance (N) that does not cause a cross-link; and the height of each above-mentioned storage node electrode is lower than a set height by approximately the value of the first length divided by two.

3. A method for manufacturing the semiconductor memory device, characterized by the fact that in a method for manufacturing the semiconductor memory device, it includes a step that forms an interlayer insulating film having storage node contacts on a semiconductor substrate, a step that forms a sacrificial film in the upper part of the above-mentioned interlayer insulating film, a step that forms openings by etching the sacrificial film so that the above-mentioned /10 storage node contacts can be exposed, a step that forms an electroconductive layer in the above-mentioned openings and on the surface of the sacrificial film, a step that chemically and mechanically polishes the above-mentioned electroconductive layer to expose the sacrificial film surface, and a step that forms storage node electrodes by etching the electroconductive layer up to a prescribed length; at the step that forms the above-mentioned openings, the gap between the openings is maintained to the degree that a first length (X) is subtracted from the minimum length that does not cause a cross-link between the storage node electrodes; and at the step that etches the above-mentioned electroconductive layer up to a prescribed length, the electroconductive layer is etched to the degree of the first length divided by two.

4. A method for manufacturing the semiconductor memory device, characterized by the fact that in a method for manufacturing the semiconductor memory device, it includes a step that forms an interlayer insulating film having storage node contacts on a semiconductor substrate, a step that sequentially forms first and second sacrificial films with different wet-etching rates in the upper part of the above-mentioned interlayer insulating film, a step that forms a first opening by anisotropically etching the first and second sacrificial films so that the above-mentioned

storage node contacts can be exposed, a step that forms a second opening whose diameter is widened toward the upper part by wet-etching the above-mentioned first and second sacrificial films, a step that forms an electroconductive layer in the above-mentioned second opening and on the surface of the sacrificial films, a step that chemically and mechanically polishes the above-mentioned electroconductive layer to expose the sacrificial film surfaces, and a step that forms storage node electrodes by etching the electroconductive layer up to a prescribed length; the shortest gap between the above-mentioned second opening is maintained to the degree that a first length (X) is subtracted from the minimum distance that does not cause a cross-link between the storage node electrodes; and at the step that etches the above-mentioned electroconductive up to a prescribed length, the electroconductive layer is etched to the degree of the first length divided by two.

5. The method for manufacturing the semiconductor memory device of Claim 4, characterized by the fact that the above-mentioned second sacrificial film has an excellent wet-etching selection ratio, compared with the above-mentioned first sacrificial film.

6. The method for manufacturing the semiconductor memory device of Claim 5, characterized by the fact that the above-mentioned first sacrificial film is vapor-deposited while applying a plasma vapor-deposition power of 250-300 W; and the above-mentioned second sacrificial film is vapor-deposited while applying the plasma vapor-deposition power (W) of about 100-150 W.

7. The method for manufacturing the semiconductor memory device of Claim 5, characterized by the fact that the above-mentioned first sacrificial film is vapor-deposited at a temperature of 400-450°C; and the above-mentioned second sacrificial film is vapor-deposited at a temperature of 270-300°C.

8. The method for manufacturing the semiconductor memory device of Claim 5, /11
characterized by the fact that the above-mentioned first sacrificial film is vapor-deposited by regulating the ratio of a nitric acid gas to a silane gas to 0.02-0.03%; and the second sacrificial film is vapor-deposited by regulating the ratio of the nitric acid gas to the silane gas to 0.05-0.06%.

9. The method for manufacturing the semiconductor memory device of Claim 5, characterized by the fact that the above-mentioned first sacrificial film is vapor-deposited by regulating the distance between a shower head of a vapor deposition equipment and the substrate to 220-250 mils; and the second sacrificial film is vapor-deposited by regulating the distance between the shower head and the substrate to 400-450 mils.

10. The method for manufacturing the semiconductor memory device of Claim 5, characterized by the fact that the above-mentioned first sacrificial film is vapor-deposited at a pressure of 1-1.5 torr; and the second sacrificial film is vapor-deposited at a pressure of 3-5 torr.

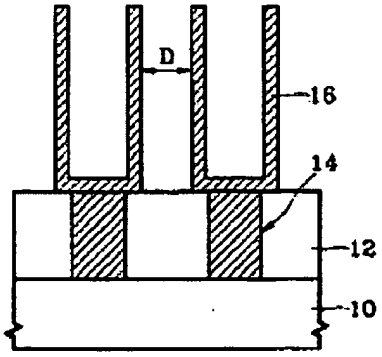

Figure 1

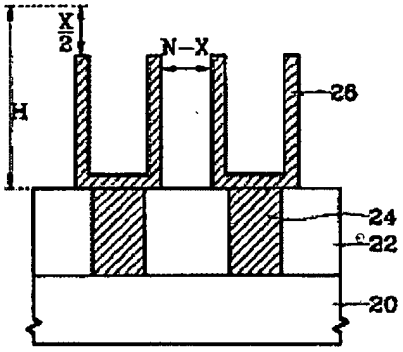

Figure 2

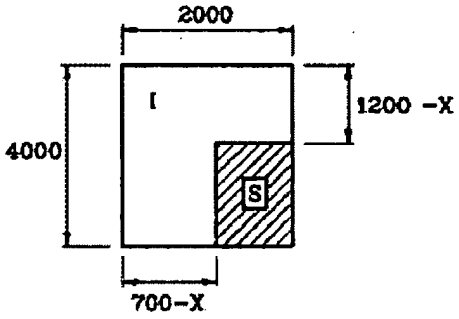

Figure 3a

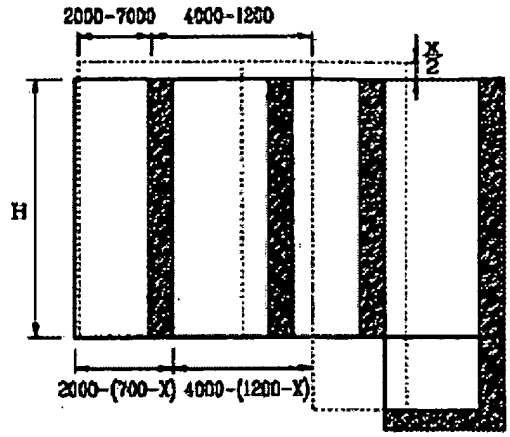

Figure 3b

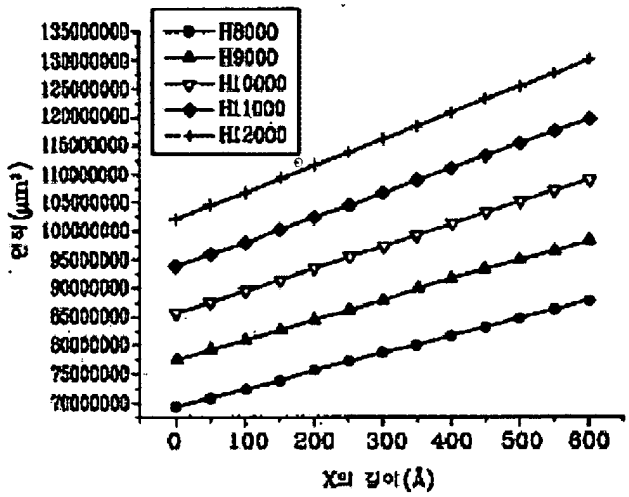

Figure 4

Key: 1 Area (μm^2)
2 Length of X (Å)

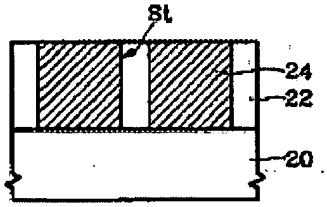

Figure 5a

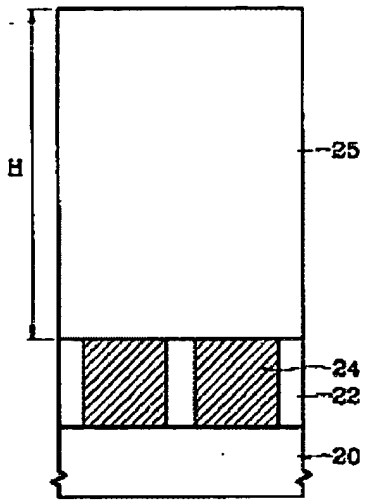

Figure 5b

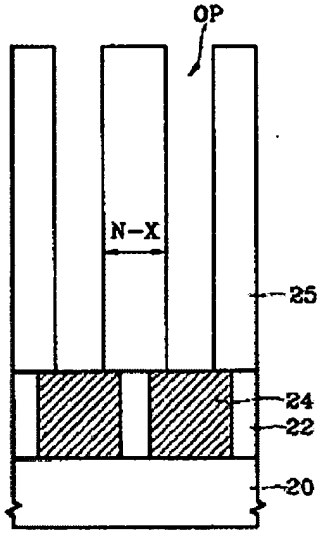

Figure 5c

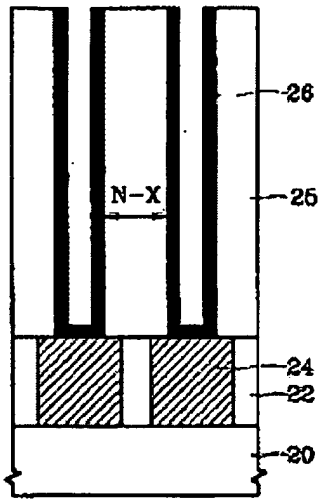

Figure 5d

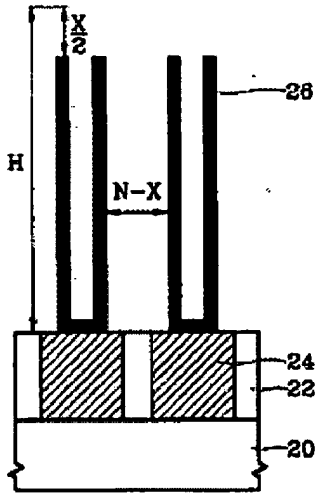

Figure 5e

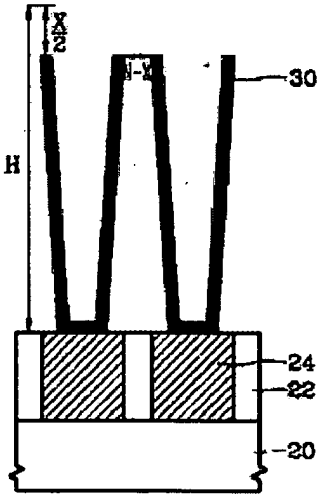

Figure 6

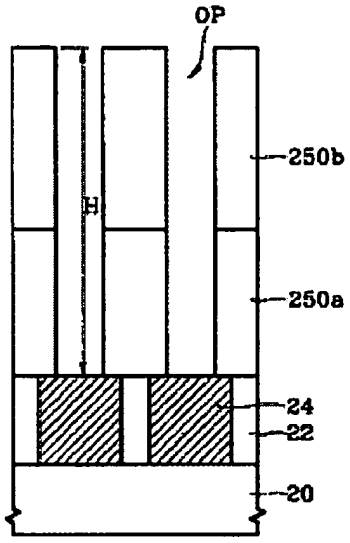

Figure 7a

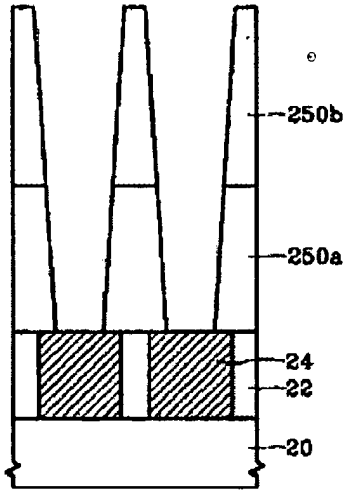

Figure 7b

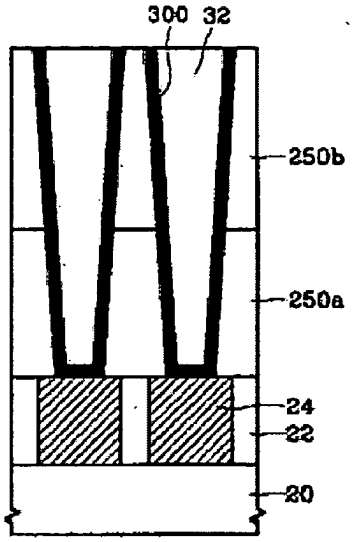

Figure 7c

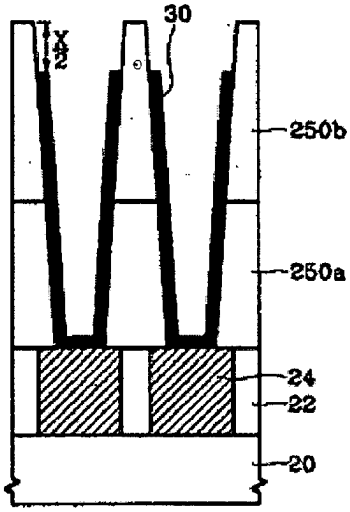

Figure 7d

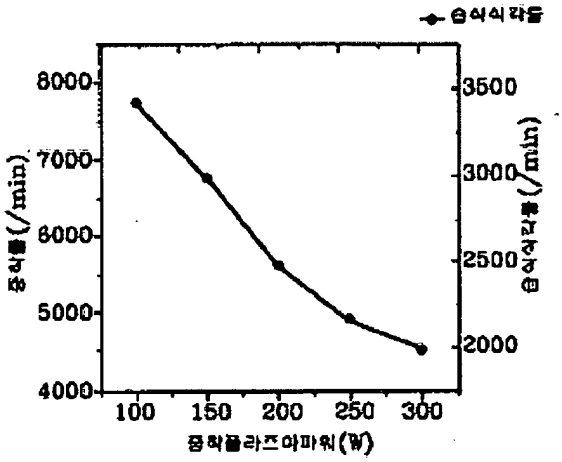

Figure 8a

Key: 1 Vapor deposition rate (/min)
2 Vapor deposition plasma power (W)
3 Wet-etching rate
4 Wet-etching rate (/min)

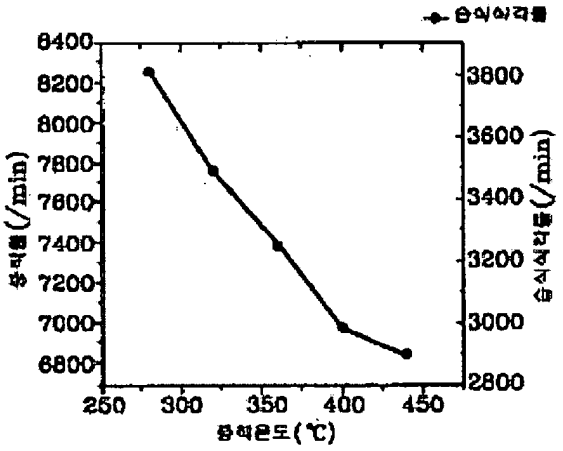

Figure 8b

Key: 1 Vapor deposition rate (/min)
2 Vapor deposition temperature (°C)
3 Wet-etching rate
4 Wet-etching rate (/min)

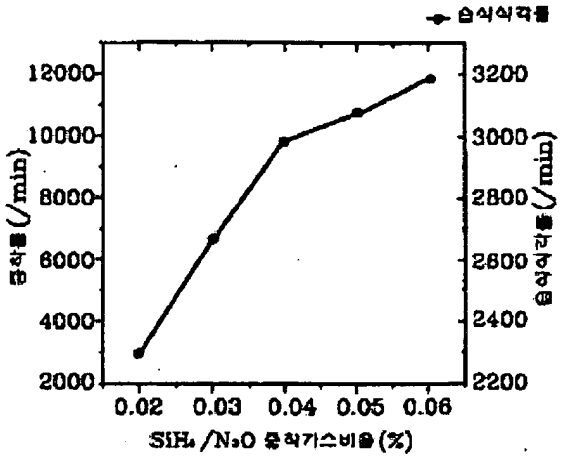

Figure 8c

Key: 1 Vapor deposition rate (/min)
2 SiH_4/N_2O vapor-depositing gas ratio (%)
3 Wet-etching rate
4 Wet-etching rate (/min)

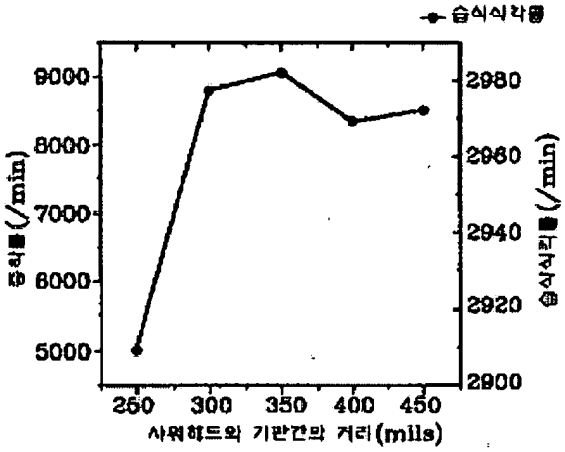

Figure 8d

Key: 1 Vapor deposition rate (/min)
2 Distance between the shower head and the substrate (mils)
3 Wet-etching rate
4 Wet-etching rate (/min)

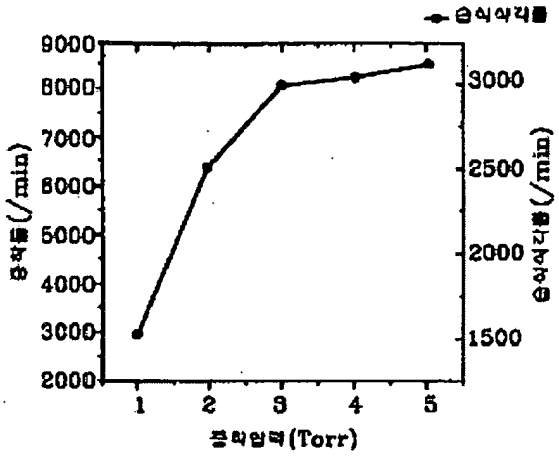

Figure 8e

Key: 1 Vapor deposition rate (/min)
2 Vapor deposition pressure (Torr)
3 Wet-etching rate
4 Wet-etching rate (/min)